Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for recovering data, comprising:

sampling a serial data stream to generate sampled data bits;

comparing sampled data bits to detect an edge transition; and

reducing false locks by setting a size of increase or decrease of a phase shift based on a zone in which the edge transition is detected, the size being set to a first value if the zone is a lock zone and to a second value if the zone is a far-to-lock zone.

2. (Original) The method of claim 1, further comprising:

continuously maintaining the size of increase or decrease of the phase shift to the second value if the edge transition is continuously detected in the far-to-lock zone.

3. (Original) The method of claim 1, further comprising:

adjusting the second value based on a number of consecutive times that the far-to-lock zone is set.

4. (Original) The method of claim 1, further comprising:

storing the sampled data bits;

generating directives; and

selecting relevant directives based on one of a plurality of rates of the serial data stream.

5. (Original) The method of claim 1, further comprising:

selecting a set of a plurality of sampling points based on one of a plurality of rates of the serial data stream.

6. (Original) The method of claim 5, further comprising:

generating a clock;

generating a plurality phase shifted clocks based on the clock; and

selecting an edge of each of one or more of the phase shifted clocks as the plurality of sampling points.

7. (Original) The method of claim 6, further comprising:

sampling the serial data stream at the sampling points;

comparing consecutive samples of the serial data stream to generate compare results; and

changing a phase shift of the phase shifted clocks based on the compare results.

8. (Original) The method of claim 6, further comprising:

setting a clock rate of the clock to be at a selected rate;

selecting two sampling points for a rate of the serial data stream that is twice the selected rate; and

selecting four sampling points for rates of the serial data stream that are equal to or less than the selected rate.

9. (Original) The method of claim 8, further comprising:

selecting an edge of each of two phase shifted clocks to be the sampling points for a rate of the serial data stream that is half the selected rate; and

selecting an edge of one of the phase shifted clocks to be the sampling points for a rate of the serial data stream that is one quarter of the selected rate.

10. (Currently Amended) An apparatus to recover data, comprising:

a sampler that samples a serial data stream to generate sampled data bits;

at least one comparator that compares sampled data bits to detect an edge transition; and

a controller that ~~sets~~ reduces false locks by setting a size of increase or decrease of a phase shift based on a zone in which the edge transition is detected, the size being set to a first value if the zone is a lock zone and to a second value if the zone is a far-to-lock zone.

11. (Original) The apparatus of claim 10, wherein

the controller continuously maintains the size of increase or decrease of the phase shift to the second value if the edge transition is continuously detected in the far-to-lock zone.

12. (Original) The apparatus of claim 10, wherein

the controller adjusts the second value based on a number of consecutive times that the far-to-lock zone is set.

13. (Original) The apparatus of claim 10, further comprising:

at least one memory that stores the sampled data bits; and

a directive extractor that extracts directives from the sampled data bits; and

a directive selector that selects relevant directives based on one of a plurality of rates of the serial data stream.

14. (Original) The apparatus of claim 10, further comprising:

a selector that selects a set of a plurality of sampling points based on one of a plurality of rates of the serial data stream.

15. (Original) The apparatus of claim 14, further comprising:

a clock generator that generates a clock;

at least one phase rotator that generates a plurality phase shifted clocks based on the clock, wherein an edge of each of one or more of the phase shifted clocks are used as the plurality of sampling points.

16. (Original) The apparatus of claim 15, wherein

the sampler samples the serial data stream at the sampling points;

the comparator compares consecutive samples of the serial data stream to generate compare results; and

the controller causes a phase shift of the phase shifted clocks based on the compare results.

17. (Original) The apparatus of claim 15, wherein

the selector selects two sampling points for a rate of the serial data stream that is twice a selected clock rate of the clock generator; and

the selector selects four sampling points for rates of the serial data stream that are equal to or less than the selected rate of the clock generator.

18. (Original) The apparatus of claim 17, wherein

the selector selects an edge of each of two phase shifted clocks to be the sampling points for a rate of the serial data stream that is half the selected rate; and

the selector selects an edge of one of the phase shifted clocks to be the sampling points for a rate of the serial data stream that is one quarter of the selected rate.

19. (Original) A system or network that includes the apparatus of claim 10.

20. (Currently Amended) An apparatus to recover data, comprising:

means for sampling a serial data stream to generate sampled data bits;

means for selecting relevant sampled data bits based on one of a plurality of rates of the serial data stream;

means for comparing sampled data bits to detect an edge transition; and

means for reducing false locks by setting a size of increase or decrease of a phase shift based on a zone in which the edge transition is detected, the size being set to a first value if the zone is a lock zone and to a second value if the zone is a far-to-lock zone.

21. (New) A method for recovering data by reducing false locks, comprising:

sampling a serial data stream to generate sampled data bits;

locating the data edge during a lock acquisition to accelerate the data edge by increasing or decreasing the size of a phase shift;

comparing sampled data bits to detect an edge transition; and

setting a size of increase or decrease of a phase shift based on a zone in which the edge transition is detected, the size being set to a first value if the zone is a lock zone and to a second value if the zone is a far-to-lock zone.